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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/645,710 | 08/21/2003 | Michael T. Andreas | 2269-5663US<br>(02-1325.00/U | 8457 |

24247 7590 08/31/2004

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| EXAMINER | |
|---|---|
| HO, TU TU V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 08/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/645,710 | ANDREAS ET AL. | |
| | Examiner | Art Unit | |
| | Tu-Tu Ho | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *27-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/21/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Oath/Declaration*

1. The oath or declaration filed on 08/21/2003 is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: Citizenship of second joint inventor is not specified.

### *Election/ Restriction*

2. Applicant's election without traverse of Group I, claims 1-26, in reply filed 08/16/2004 is acknowledged. The requirement is still deemed proper and is made FINAL. Accordingly, claims 27-29 are withdrawn from consideration.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-26** are rejected under 35 U.S.C. §103(a) as being unpatentable over Wu et al. U.S. Patent 6,057,248 (cited by Applicant) for being obvious and further in view of Skee U.S. Patent 6,465,403 (also cited by Applicant).

Referring to **independent claims 1 and 19 and dependent claim 26**, Wu discloses a method of cleaning a semiconductor wafer including at least one registration mark (alignment mark, Abstract), comprising:

providing a semiconductor wafer comprising at least one registration mark, the at least one registration mark comprising at least one trench (groove);

exposing the semiconductor wafer to a cleaning solution ($NH_4OH$ – ammonia hydroxide – Abstract); and

exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy ("megasonic source", Abstract).

However, Wu fails to disclose a specific width for the at least one trench. Specifically, Wu fails to disclose that the at least one trench has a trench width from approximately 1.0 μm to approximately 3.0 μm. Nevertheless, a trench width from approximately 1.0 μm to approximately 3.0 μm for a trench of a registration mark, at the time the invention was made, was, as admitted in paragraph [0002] in the description of the present invention, known in the art. See also, for example, U.S. Patent 6,661,105 to Yamamoto et al., column 3, lines 46-56, which discloses a trench for a registration mark having a width from 1.0 μm to 5.0 μm. Since the claimed width was known in the art, specifying the width for the trench or forming the trench with such a width would have been obvious.

Furthermore, Wu fails to disclose that the cleaning solution comprises tetramethylammonium hydroxide and at least one surfactant, the at least one surfactant comprising at least one acetylenic diol surfactant. Instead, Wu discloses that the cleaning solution comprises ammonia hydroxide. Nevertheless, Skee, in disclosing cleaning solutions for

stripping and cleaning a semiconductor wafer substrate, teaches that a cleaning solution comprising tetramethylammonium hydroxide (TMAH) and at least one surfactant, the at least one surfactant comprising at least one acetylenic diol surfactant (column 9, lines 18-27), is more effective in removing contaminants such as organic and metal-containing residues after a typical etching process as compared with other cleaning compositions in the art (paragraph bridging columns 4 and 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expose the semiconductor wafer to a cleaning solution comprising tetramethylammonium hydroxide and at least one surfactant - the at least one surfactant comprising at least one acetylenic diol surfactant - rather than just ammonia hydroxide as disclosed by Wu. One would have been motivated to make such a modification in view of the suggestion in Skee that a cleaning solution comprising tetramethylammonium hydroxide (TMAH) and at least one surfactant - the at least one surfactant comprising at least one acetylenic diol surfactant - is more effective in removing contaminants such as organic and metal-containing residues.

Referring to the limitation "spray" and "spraying" in "contacting the semiconductor wafer with a spray of a cleaning solution" of **claim 19** and "spraying the cleaning solution on a surface of the semiconductor wafer" of **claim 18**, although Wu does not specifically disclose a manner in which the cleaning solution is applied, it is known in the art, as is disclosed by Skee in column 10, lines 62-67, that the cleaning solution is applied either by bath or spray. Since spray and bath are two known methods of introducing the cleaning solution, using either method would have been obvious to one of ordinary skill in the art at the time the invention was made.

Hereinafter, the mentioned references, which teach a method that meets the limitations of claims 1 and 19, just as detailed above, is simply referred to as the combined reference.

Referring to the limitation "organic" and "polymeric" of the particulate contaminants of **claims 2-4 and 20-22**, the combined reference (Wu) fails to disclose such materials for the particulate contaminants, however, Wu also fails to exclude the use of such materials. It is known in the art of semiconductor that the materials used for interlevel dielectric layers (ILD) are either inorganic, organic, polymeric inorganic, or polymeric organic materials, which materials become particulate contaminants after the normal processing of semiconductor wafers. Since Wu does not exclude the use of the claimed materials, the use of the claimed materials in the process of the combined reference would have been obvious.

Referring to **claims 5-6 and 23-24**, as detailed above, the claimed width was known in the art.

With respect to the limitations "approximately 0.01 by weight to approximately 25% by weight tetramethylammonium hydroxide" for the cleaning solution of **claim 7**, the combined reference discloses 0.1-2% by weight tetramethylammonium hydroxide for the cleaning solution (Skee, column 9, lines 18-21). Although the Skee's weight range only overlaps the claimed weight range, the change from one weight range to the other would have been obvious because: 1) it appears that it is within the skill of one in the art at the time the invention was made to change the range from one to the other, or 2) both ranges are effective at contributing to removing residues.

Referring to the limitations "cleaning solution having a pH greater than approximately 7.5", "cleaning solution having a pH greater than approximately 9", and "cleaning solution

having a pH greater than approximately 10" of **claims 8-10** respectively, the combined reference discloses a cleaning solution having a pH of about 11 or greater (Skee, column 5, lines 35-40). Although the Skee's range of the pH level only overlaps the claimed range, the change from one pH level to the other would have been obvious because: 1) it appears that it is within the skill of one in the art at the time the invention was made to change the pH level from one to the other, or 2) the different pH levels are all effective at contributing to removing residues.

Referring to **claims 11 and 12**, the combined reference discloses exposing the semiconductor wafer to a cleaning solution comprising tetramethylammoniurn hydroxide and at least one surfactant comprising exposing the semiconductor wafer to a cleaning solution comprising tetramethylammonium hydroxide and Surfynol® 465, a non-ionic surfactant (Skee, column 11, lines 43-48). In other word, the combined reference discloses a method as claimed but instead of disclosing Surfynol® CT-131 - a non-ionic surfactant as claimed, it discloses Surfynol® 465, a non-ionic surfactant. However, the change from one non-ionic surfactant to the other non-ionic surfactant would have been obvious because: 1) it appears that it is within the skill of one in the art at the time the invention was made to change from one non-ionic surfactant to the other non-ionic surfactant, or 2) both of the non-ionic surfactants are effective at contributing to removing organic residues. The materials list for the surfactant of **claim 12**, as noted by Applicant, is that of Surfynol® CT-131. Surfynol® CT-131 and Surfynol® 465 are various surfactants produced by Air Products and Chemicals, Inc., as noted by Applicant and Skee, respectively.

Referring to **claim 13**, as noted above, the combined reference further discloses that exposing the semiconductor wafer to a cleaning solution comprising tetramethylammonium

hydroxide and at least one surfactant comprises immersing (bath) the semiconductor wafer in the cleaning solution.

Referring to **claim 14**, the combined reference further discloses that exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy comprises exposing the semiconductor wafer to a vibrational energy ranging from approximately 40 kHz to approximately 104 kHz (Wu, ultrasonic source, column 2, lines 38-53).

Referring to **claim 15**, the combined reference further discloses that exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy comprises exposing the semiconductor wafer to a vibrational energy ranging from approximately 850 kHz to approximately 1.5 MHz. (Wu, megasonic source, column 2, lines 38-53).

Referring to **claim 16**, the combined reference further discloses exposing the semiconductor wafer to a temperature ranging from approximately 25°C to approximately 65°C (Skee, column 10, lines 64-67).

Referring to **claim 17**, the combined reference further discloses exposing the semiconductor wafer to a temperature ranging from approximately 55°C to approximately 65°C (Skee, column 10, lines 64-67).

Referring to **claim 25**, as noted above, the combined reference discloses contacting the semiconductor wafer with a spray of a cleaning solution comprising tetramethylammonium hydroxide and at least one surfactant comprises contacting the semiconductor wafer with a spray. However, the reference fails to explicitly disclose that contacting the semiconductor wafer with the spray comprises contacting the semiconductor wafer with a high-pressure jet spray or a high-velocity aerosol spray. Nevertheless, the spray should be delivered by a nozzle, rather than by

hand, as is known in the art, which nozzle would necessarily produce a rather high-pressure or high-velocity spray. Since the limitation high-pressure and high-velocity are either inherent or obvious variants, the limitations would have been obvious to one of ordinary skill in the art at the time the invention was made.

4. **Claims 1-26** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chen U.S. Patent Application Publication 20040132384 in view of Skee and further in view of Wu and knowledge in the art.

Chen discloses in the Abstract, paragraph [0004], and paragraph [0006] a method for cleaning organic residue of alignment marks on a CMP polished wafer.

In particular, and with reference to **independent claims 1 and 19 and dependent claims 2, 4, 20, and 22**, Chen discloses a method of cleaning a semiconductor wafer including at least one registration mark (alignment mark) having a trench (paragraph [0004] contaminated with organic particles (organic residues) and a cleaning solution as claimed. However, Chen fails to disclose a width for the trench of the registration mark as claimed, fails to disclose that the cleaning solution comprises tetramethylammonium hydroxide and at least one surfactant of acetylenic diol, and fails to disclose exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy as claimed.

As for the limitation the cleaning solution comprising tetramethylammonium hydroxide and at least one surfactant of acetylenic diol, Skee discloses such a solution for such a purpose as detailed above in paragraph numbered 3. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a solution comprising

tetramethylammonium hydroxide and at least one surfactant of acetylenic diol instead of the solution disclosed by Chen for removing organic residues. One would have been motivated to make such a modification in view of the suggestion in Skee that a cleaning solution comprising tetramethylammonium hydroxide (TMAH) and at least one surfactant - the at least one surfactant comprising at least one acetylenic diol surfactant - is effective in removing organic contaminants (paragraph bridging columns 4 and 5).

As for the limitation exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy, Wu teaches in column 2, lines 38-53 that during the step of exposing the semiconductor wafer to the cleaning solution, an ultrasonic or megasonic vibrational energy is applied to the semiconductor wafer to effectively remove different kinds of contamination particles. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy. One would have been motivated to make such a modification in view of the teachings of Wu that exposing the semiconductor wafer to an ultrasonic or megasonic vibrational energy facilitates removing different kinds of contamination particles.

As for the claimed width of the trench, as detailed above in paragraph numbered 3, the width is known in the art. Therefore, specifying the width for the trench or forming the trench with such a width would have been obvious at the time the invention was made.

Hereinafter, the mentioned references, including which that discloses general knowledge in the art, which teach a method that meets the limitations of claims 1 and 19, just as detailed above, is simply referred to as the combined reference.

Referring to the limitation "polymeric" of the particulate contaminants of **claims 3 and 21**, the combined reference fails to disclose such materials for the particulate contaminants, however, the combined reference also fails to exclude the use of such materials. It is known in the art of semiconductor that the materials used for interlevel dielectric layers (ILD) are either inorganic, organic, polymeric inorganic, or polymeric organic materials, which materials become particulate contaminants after the normal processing of semiconductor wafers. Since the combined reference does not exclude the use of the claimed materials, the use of the claimed materials in the process of the combined reference would have been obvious.

Referring to **claims 5-6 and 23-24**, as detailed above, the claimed width was known in the art.

With respect to the limitations "approximately 0.01 by weight to approximately 25% by weight tetramethylammonium hydroxide" for the cleaning solution of **claim 7**, the combined reference discloses 0.1-2% by weight tetramethylammonium hydroxide for the cleaning solution (Skee, column 9, lines 18-21). Although the Skee's weight range only overlaps the claimed weight range, the change from one weight range to the other would have been obvious because: 1) it appears that it is within the skill of one in the art at the time the invention was made to change the range from one to the other, or 2) both ranges are effective at contributing to removing organic residues.

Referring to the limitations "cleaning solution having a pH greater than approximately 7.5", "cleaning solution having a pH greater than approximately 9", and "cleaning solution having a pH greater than approximately 10" of **claims 8-10** respectively, the combined reference discloses a cleaning solution having a pH of about 11 or greater (Skee, column 5, lines 35-40).

Although the Skee's range of the pH level only overlaps the claimed range, it appears that the change from one pH level to the other would have been obvious because: 1) it appears that it is within the skill of one in the art at the time the invention was made to change the pH level from one to the other, or 2) the different pH levels are all effective at contributing to removing organic residues.

Referring to **claims 11 and 12**, the combined reference discloses exposing the semiconductor wafer to a cleaning solution comprising tetramethylammoniurn hydroxide and at least one surfactant comprising exposing the semiconductor wafer to a cleaning solution comprising tetramethylammonium hydroxide and Surfynol® 465, a non-ionic surfactant (Skee, column 11, lines 43-48). In other word, the combined reference discloses a method as claimed but instead of disclosing Surfynol® CT-131 - a non-ionic surfactant as claimed, it discloses Surfynol® 465, a non-ionic surfactant. However, the change from one non-ionic surfactant to the other non-ionic surfactant would have been obvious because: 1) it appears that it is within the skill of one in the art at the time the invention was made to change from one non-ionic surfactant to the other non-ionic surfactant, or 2) both of the non-ionic surfactants are effective at contributing to removing organic residues. The material list for the surfactant of **claim 12**, as noted by Applicant, is that of Surfynol® CT-131. Surfynol® CT-131 and Surfynol® 465 are various surfactants produced by Air Products and Chemicals, Inc., as noted by Applicant and Skee, respectively.

Referring to **claim 13**, as noted above, the combined reference further discloses that exposing the semiconductor wafer to a cleaning solution comprising tetramethylammonium

hydroxide and at least one surfactant comprises immersing (bath) the semiconductor wafer in the cleaning solution.

Referring to **claim 14**, the combined reference further discloses that exposing the semiconductor wafer to ultrasonic or megasonic vibrational energy comprises exposing the semiconductor wafer to a vibrational energy ranging from approximately 40 kHz to approximately 104 kHz (Wu, ultrasonic source, column 2, lines 38-53).

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Referring to **claim 16**, the combined reference further discloses exposing the semiconductor wafer to a temperature ranging from approximately 25°C to approximately 65°C (Skee, column 10, lines 64-67).

Referring to **claim 17**, the combined reference further discloses exposing the semiconductor wafer to a temperature ranging from approximately 55°C to approximately 65°C (Skee, column 10, lines 64-67).

Referring to **claim 25**, as noted above, the combined reference discloses contacting the semiconductor wafer with a spray of a cleaning solution comprising tetramethylammonium hydroxide and at least one surfactant comprises contacting the semiconductor wafer with a spray. However, the reference fails to explicitly disclose that contacting the semiconductor wafer with the spray comprises contacting the semiconductor wafer with a high-pressure jet spray or a high-velocity aerosol spray. Nevertheless, the spray should be delivered by a nozzle, rather than by

hand, as is known in the art, which nozzle would necessarily produce a rather high-pressure or high-velocity spray. Since the limitation high-pressure and high-velocity are either inherent or obvious variants, the limitations would have been obvious to one of ordinary skill in the art at the time the invention was made.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
August 27, 2004